

LINDBLOM et al
Serial No. 09/688,165

Atty Dkt: 2380-155
Art Unit: 2661

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A cell switch comprising:
a first switch plane comprising a first switch core;
a second switch plane comprising a second switch core;
a sender switch port interface unit;
a receiver switch port interface unit;
wherein the sender switch port interface unit sends maintenance cells to the receiver switch port interface unit by sending first plane maintenance cells via the first switch plane but not via the second switch plane and by sending second plane maintenance cells via and the second switch plane but not via the first switch plane, the first plane maintenance cells being applied to the first switch plane and the second plane maintenance cells being applied to the second switch plane in a predetermined sequence, each of the first plane maintenance cells and the second plane maintenance cells including a plane indicator which informs the receiver switch port interface unit whether the maintenance cell traveled through the first switch plane or the second switch plane;
wherein the receiver switch port interface unit detects an erroneous switch plane when the first plane maintenance cells and the second plane maintenance cells from the sender switch port interface unit do not arrive in the predetermined sequence.

2. (Currently Amended) The apparatus of claim 1, wherein the predetermined sequence comprises the first plane maintenance cells applied to the first switch plane and the second plane maintenance cells applied to the second switch plane in alternation.

3. (Cancelled)

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4. (Currently Amended) The apparatus of claim 1, wherein the sender switch port interface unit sends a cycle of maintenance cells to the receiver switch port interface unit, the cycle comprising plural sets of the predetermined sequence of the first plane maintenance cells and the second plane maintenance cells, and wherein at least a portion of the maintenance cell of one of the sets of the cycle is inverted with respect to a corresponding portion of the maintenance cell of another of the sets of the cycle.

5. (Original) The apparatus of claim 4, wherein the cycle comprises two sets of the predetermined sequence of maintenance cells.

6. (Original) The apparatus of claim 1, wherein the receiver switch port interface unit detects an erroneous switch plane by performing error checking with respect to contents of a received maintenance cell.

7. (Currently Amended) The apparatus of claim 1, further comprising N number of receiver switch port interface units, and wherein the sender switch port interface unit applies maintenance cells to the N number of receiver switch port interface units in a cycle, the cycle comprising (1) non-inverted first plane maintenance cells sent via the first switch plane to each of the N number of receiver switch port interface units; (2) non-inverted second plane maintenance cells sent via the second switch plane to each of the N number of receiver switch port interface units; (3) inverted first plane maintenance cells sent via the first switch plane to each of the N number of receiver switch port interface units; and (4) inverted second plane maintenance cells sent via the second switch plane to each of the N number of receiver switch port interface units, the inverted first plane maintenance cells and the inverted second plane maintenance cells having at least a portion thereof inverted with respect to the corresponding non-inverted cell of the cycle.

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8. (Currently Amended) A cell switch comprising:
a switch plane comprising a switch core;
a sender switch port interface unit;
a receiver switch port interface unit;
wherein the sender switch port interface unit sends a pair of maintenance cells to the receiver switch port interface unit via the switch plane, a first maintenance cell of the pair having a predetermined payload portion thereof inverted with respect to a corresponding portion of a second maintenance cell of the pair.

9. (Currently Amended) The apparatus of claim 8, further comprising a second switch plane through which the sender switch port interface unit also sends a second pair of maintenance cells to the receiver switch port interface unit, a first maintenance cell of the second pair having a predetermined payload portion thereof inverted with respect to a corresponding portion of a second maintenance cell of the second pair.

10. (Currently Amended) A cell switch comprising:
a first switch plane comprising a first switch core;
a second switch plane comprising a second switch core;
a sender switch port interface unit;
plural receiver switch port interface units, and wherein the sender switch port interface unit applies maintenance cells to the plural receiver switch port interface units in a cycle, the cycle comprising (1) non-inverted first plane maintenance cells sent via the first switch plane but not via the second switch plane to each of the plural receiver switch port interface units; (2) non-inverted second plane maintenance cells sent via the second switch plane but not via the first switch plane to each of the plural receiver switch port interface units; (3) inverted first plane maintenance cells sent via the first switch plane but not via the second switch plane to each of the plural receiver switch port interface units; and (4) inverted second plane maintenance cells sent via the second

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switch plane but not via the first switch plane to each of the plural receiver switch port interface units, each of the first plane maintenance cells and the second plane maintenance cells including a plane indicator which informs the receiver switch port interface unit whether the maintenance cell traveled through the first switch plane or the second switch plane, the inverted first plane maintenance cells and the inverted second plane maintenance cells having at least a portion thereof inverted with respect to the corresponding non-inverted cell of the cycle.

11. (Currently Amended) A method of operating a cell switch comprising:
a first switch plane comprising a first switch core;
a second switch plane comprising a second switch core;
a sender switch port interface unit;
a receiver switch port interface unit;
a sender switch port interface unit which sending sends maintenance cells to a receiver switch port interface unit by sending by sending first plane maintenance cells via the first switch plane but not via the second switch plane and by sending second plane maintenance cells via the second switch plane but not via the first switch plane, and a second switch plane, each of the first plane maintenance cells and the second plane maintenance cells including a plane indicator which informs the receiver switch port interface unit whether the maintenance cell traveled through the first switch plane or the second switch plane, the first plane maintenance cells and the second plane maintenance cells being respectively applied to the first switch plane and the second switch plane in a predetermined sequence;

detecting, at the receiver switch port interface unit, an erroneous switch plane when the first plane maintenance cells and the second plane maintenance cells from the sender switch port interface unit do not arrive in the predetermined sequence.

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12. (Currently Amended) The method of claim 11, further comprising forming the predetermined sequence by alternating application of the first plane maintenance cells to the first switch plane and of the second plane maintenance cells to the second switch plane.

13. (Currently Amended) The method of claim 11, further comprising including in the maintenance cell a plane indicator and using the plane indicator at the receiver switch port interface unit to determine whether the maintenance cell traveled through the first switch plane or the second switch plane.

14. (Currently Amended) The method of claim 11, further comprising sending a cycle of maintenance cells to the receiver switch port interface unit, the cycle comprising plural sets of the predetermined sequence of the first plane maintenance cells and the second plane maintenance cells, and wherein at least a portion of the maintenance cells of one of the sets of the cycle is inverted with respect to a corresponding portion of the maintenance cells of another of the sets of the cycle.

15. (Currently Amended) The method of claim 14, further comprising forming the cycle with two sets of the predetermined sequence of first plane maintenance cells and second plane maintenance cells.

16. (Original) The method of claim 11, further comprising detecting at the receiver switch port interface unit an erroneous switch plane by performing error checking with respect to contents of a received maintenance cell.

17. (Currently Amended) The method of claim 11, further comprising the sender switch port interface unit applying maintenance cells to N number of receiver switch port interface units in a cycle, the cycle comprising (1) non-inverted first plane maintenance

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cells sent via the first switch plane to each of the N number of receiver switch port interface units; (2) non-inverted second plane maintenance cells sent via the second switch plane to each of the N number of receiver switch port interface units; (3) inverted first plane maintenance cells sent via the first switch plane to each of the N number of receiver switch port interface units; and (4) inverted second plane maintenance cells sent via the second switch plane to each of the N number of receiver switch port interface units, the inverted maintenance cells having at least a portion thereof inverted with respect to the corresponding non-inverted cell of the cycle.

18. (Currently Amended) A method of operating a cell switch comprising sending a pair of maintenance cells from a sender switch port interface unit to a receiver switch port interface unit via a switch plane, a first maintenance cell of the pair having a predetermined payload portion thereof inverted with respect to a corresponding portion of a second maintenance cell of the pair.

19. (Currently Amended) The method of claim 18, further comprising sending a second pair of maintenance cells via a second switch plane to the receiver switch port interface unit, a first maintenance cell of the second pair having a predetermined payload portion thereof inverted with respect to a corresponding portion of a second maintenance cell of the second pair.

20. (Currently Amended) A method of operating a cell switch comprising applying maintenance cells from a sender switch port interface unit to plural receiver switch port interface units in a cycle, the cycle comprising (1) non-inverted first plane maintenance cells sent via a first switch plane but not via a second switch plane to each of the plural receiver switch port interface units; (2) non-inverted second plane maintenance cells sent via the second switch plane but not via the first switch plane to each of the plural receiver switch port interface units; (3) inverted first plane

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maintenance cells sent via the first switch plane but not via the second switch plane to each of the plural receiver switch port interface units; and (4) inverted second plane maintenance cells sent via the second switch plane but not via the first switch plane to each of the plural receiver switch port interface units, each of the first plane maintenance cells and the second plane maintenance cells including a plane indicator which informs the receiver switch port interface unit whether the maintenance cell traveled through the first switch plane or the second switch plane, the inverted first plane maintenance cells and second plane maintenance cells having at least a portion thereof inverted with respect to the corresponding non-inverted cell of the cycle.

[PLEASE ADD NEW CLAIMS 21 – 24 AS FOLLOWS:]

21. (New) The apparatus of claim 8, wherein the payload portion of the first maintenance cell of the pair is a bit pattern which tests a cross-point buffer memory of the switch core.

22. (New) The apparatus of claim 9, wherein the payload portion of the first maintenance cell of the second pair is a bit pattern which tests a cross-point buffer memory of the switch core.

23. (New) The method of claim 18, wherein the payload portion of the first maintenance cell of the pair is a bit pattern which tests a cross-point buffer memory of the switch core.

24. (New) The method of claim 19, wherein the payload portion of the first maintenance cell of the second pair is a bit pattern which tests a cross-point buffer memory of the switch core.